What is Claimed is:

[c1] A circuit used in modeling integrated circuits, which comprises:

a first current source connecting an output node to a voltage supply; and
a second current source connecting an the output node to a ground;
a Miller capacitor connected to an input node and the output node;
an input capacitor connected to the input node and to ground; and
an output capacitor and internal impedance, Zint, connected to the output node and ground.

[c2] The circuit of claim 1 where the current sources are full functions of the input and output voltages.

[c3] The circuit of claim 2 where the capacitance of each capacitor and the impedance of Zint are assumed to be full functions of the input and output voltage.

[c4] The circuit of claim 1, which has an output load, Zload, which comprises three elements a near capacitor, a resistor and a far capacitor..

[c5] The circuit of claim 3 where the first current source represents the p transistor and the second current represents the n transistor.

[c6] The circuit of claim 5 where a current source when there are multiple inputs.

[c7] The circuit of claim 5 where each current source could be spit up into an arbitrary number of parallel current sources, each of which could depend on a different set of inputs, in addition to the output of interest.

[c8] A circuit used in modeling integrated circuits, which comprises:

an ideal current source connecting an output node to a voltage supply;
a Miller capacitor connected to an input node and the output node;
an input capacitor connected to the input node and to ground; and
an output capacitor and internal impedance, Zint, connected to the output node and ground.

[c9]

The circuit of claim 8 where the ideal current source is a full function of the

input and output voltages and where the capacitance of each capacitor and the impedance of Zint are assumed to be full functions of the input and output voltage.

[c10] The circuit of claim 9, which has an output load, Zload, which comprises a near capacitor, a resistor and a far capacitor.

[c11] A method of modeling an IC that provides output waveforms, comprising the steps of:

translating a model of the IC comprising ideal current sources and capacitors into a differential equation which is implicit with respect to output voltages;

supplying values of the model's elements at a sufficient I/O voltages to cover the desired range of I/O node voltages;

resimulating the model by solving the differential equation through an ODE solver, given an input waveform, the element values and an output load.

[c12] The method of modeling an IC of claim 11 also comprising the step of:

storing generalization equations and solving the generalization equations to obtain model element values.

[c13] The method of modeling an IC of claim 11 also comprising the step of:

performing measurements in order to obtain the model element values.

[c14] The method of claim 11 also comprising the steps of:

interpolating of element values in the space of I/O node voltages;

manipulating element values such as time or voltage-threshold-based delay, averaging or clipping.

[c15] The method of claim 12 also comprising the step of:

solving the generalization equations using interpolated parameters and externally specified environmental parameters to obtain model element values.

[c16]

The method of claim 11 also comprising the step of:

at each time step during solution of the ODE, determining the output load by having the ODE solver call a callback function requesting the load current by providing to the callback function the time and output node voltage.

[c17] A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for modeling an IC, the method steps comprising:

translating a model of the IC comprising ideal current sources and capacitors into a differential equation which is implicit with respect to output voltages;

supplying values of the model's elements at a sufficient I/O voltages to cover the desired range of I/O node voltages;

re-simulating the model by solving the differential equation through an ODE solver, given an input waveform, the element values and an output load.

[c18] The program storage device of claim 17 wherein the method steps also comprise:

storing generalization equations and solving the generalization equations to obtain model element values.

[c19] The program storage device of claim 17 wherein the method steps also comprise:

performing measurements in order to obtain the model element values.

[c20] The program storage device of claim 17 wherein the method steps also comprise:

interpolating of element values in the space of I/O node voltages;

manipulating element values for environmental parameters such as time or voltage-threshold-based delay, averaging, or clipping.

[c21] The program storage device of claim 18 wherein the method steps also comprise:

solving the generalization equations using interpolated parameters and

externally specified environmental parameters to obtain model element values.

[c22] The program storage device of claim 17 wherein the method steps also comprise:

at each time step of the input waveform, determining the output load by having the ODE solver call a callback function requesting the load current by providing to the callback function the time and output node voltage.